REMARKS

Claims 55-78, and 85-89 remain in this application. Claims 79-84 have been cancelled without prejudice. Claims 55, 58-59, 62-63, 66-69, 71, 74-75, 78, and 81 have been amended. The above amendments to the claims have not been made within view to overcoming any prior art of which the Applicant is aware, or that has been cited in the present Office Action. The above amendments have been made with a view to modifying the form of the claims. Claims 85-89 have been added. The amended claims and the added claims are supported by the specification and no new matter has been added. The Applicant(s) respectfully requests reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §103 Rejection – Gates in view of Carlsson

The Examiner has rejected claims 55-59, 62 and 66-84 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,701,409 issued to Gates (hereinafter referred to as "Gates") in view of U.S. Patent No. 4,053,947 issued to Carlsson ("Carlsson"). The Applicant(s) respectfully submits that the present claims are allowable over any combination of Gates and Carlsson.

Claim 75 recites a method comprising at least, "detecting a bug of the component by determining an incorrect response of the component to the predefined sequence of bus transactions". These limitations are not taught by any combination of <u>Gates</u> and <u>Carlsson</u>.

Gates does not teach or suggest detecting a bug of the component by determining an incorrect response to the predefined sequence of bus transactions. Gates discusses using a single error command to generate an error on a bus. As stated in Gates, "[t]o test the PCI bus, a device on the PCI bus loads an error command into a command register of

Docket No: 42P4788

Application No: 08/992,222

the bus error generation circuit of the integrated circuit via the PCI bus" (column 2, lines 39-42). The error command generates an error by forcing the bus error generation circuit to invert a parity bit. As stated in Gates, "[a]fter a particular error command is loaded into the command register ... the bus error generation circuit causes an incorrect parity value to be output onto the PCI bus terminal PAR during a subsequent data write PCI bus cycle" (column 2, lines 49-53). An example of this is discussed at column 4, lines 37-42. In any event, the error is generated based on a single error command and there is no teaching or suggestion to detect a bug by determining an incorrect response to a predefined sequence of bus transactions.

The limitations that are not taught or suggested by <u>Gates</u> are also not taught or suggested by <u>Carlsson</u>. <u>Carlsson</u> does not teach or suggest detecting bugs, let alone detecting bugs by determining an incorrect response to a predefined sequence of bus transactions. Accordingly, any combination of <u>Gates</u> and <u>Carlsson</u> does not teach or suggest the claims limitations. It should be noted that the Applicants are not admitting that <u>Gates</u> and <u>Carlsson</u> may be combined. In fact, it does not seem appropriate to combine <u>Gates</u> and <u>Carlsson</u>, since there is no suggestion, either express or implied, that they be combined, or that they be combined in the manner suggested. However at this time the Applicant(s) elect to point out the significant differences between the proposed combination of <u>Gates</u> and <u>Carlsson</u>.

For the foregoing reasons, Applicant(s) submits that the Examiner has failed to establish a prima facie case of obviousness set forth in MPEP Section 706.02(j). Specifically, the Examiner has failed to show that "the prior art reference (or references when combined) must teach or suggest all the claim limitations", as required by In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Docket No: 42P4788 Application No: 08/992,222 For at least these reasons, claim 75 is believed to be allowable over any

combination of Gates and Carlsson. Claims 76-78 depend from claim 75 and are

believed to be allowable therefor, as well as for the recitations independently set forth

therein.

Claims 55, 69, and 72 each recite at least, "a predefined sequence of bus

Accordingly, as discussed above, these claims are believed to be transactions".

allowable for at least the reason that any combination of Gates and Carlsson does not

teach or suggest using a predefined sequence of bus transactions. Claims 56-65 depend

on claim 55, claims 70-71 depend on claim 69, and claims 73-74 depend on claim 72.

These dependent claims are believed to be allowable therefor, as well as for the

recitations independently set forth therein.

Claim 66 recites at least, "a plurality of phase engines coupled between the logic

device and the connector to translate the digital logic into signals and provide the signals

to the bus, the plurality of phase engines including a system phase engine, an arbitration

phase engine, a request phase engine, a snoop/error phase engine, and a data phase

engine, the system phase engine, the arbitration phase engine, and the request phase

engine coupled with the flow portion, the snoop/error phase engine coupled with the

request portion, the data phase engine coupled with the data portion". Any combination

of Gates and Carlsson does not teach or suggest these limitations. Accordingly, claim 66

is believed to be allowable. Claims 67-68 depend on claim 66 and are believed to be

allowable therefor, as well as for the recitations independently set forth therein.

35 U.S.C. §103 Rejection - Gates

The Examiner has rejected claims 60-61 and 63-65 under 35 U.S.C. §103(a) as being

unpatentable over U.S. Patent No. 5,701,409 issued to Gates (hereinafter referred to as

"Gates"). Each of claims 60-61 and 63-65 depend from one of the independent claims

Docket No: 42P4788

Application No: 08/992,222

13

discussed above, and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

Docket No: 42P4788

Application No: 08/992,222

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably

define the subject invention over the prior art of record and are in condition for

allowance. Applicant(s) respectfully request that the rejections be withdrawn and the

claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there

remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicant(s) respectfully petitions for an extension of time to respond to the

outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary.

Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37

C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: MAy 16, 2003

Beaut E. Veuhi

Brent E. Vecchia Reg. No. 48,011

12400 Wilshire Boulevard
Seventh Floor

Los Angeles, California 90025-1030

Docket No: 42P4788

Application No: 08/992,222

15